	Application No.	Applicant(s)
Notice of Allowability	09/867,766	FUJIWARA, MAKOTO
	Examiner	Art Unit	
	Peter Poltorak	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--
All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the response received on 11/09/06 and the telephonic interview with Ramyar Farid*.

2. ☒ The allowed claim(s) is/are *1 and 5*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☒ All   b) ☐ Some*   c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the
         International Bureau (PCT Rule 17.2(a)).
    * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
        1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____ .
    (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of
      Paper No./Mail Date _____ .
  Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *12/11/06* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____ .

DETAILED ACTION

1. This Office Action is in response to Applicant's amendment filed on 11/09/06.

2. Claims 1 and 2 have been amended.

Examiner Amendment

3. An Examiner's Amendment to the record appears below. Should the changes

and/or additions be unacceptable to Applicant, an amendment may be filed as

provided by 37 CFR 1.312. To ensure consideration of such an amendment, it

MUST be submitted no later than the payment of the Issue Fee.

The following changes were authorized (and permission to make same by

Authorization for this Examiner's Amendment was given in a telephone interview

with Ramyar Farid on 12/11/06).

4. Please amend claims 1 and 5 as follows:

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1. A semiconductor integrated circuit comprising:

        a ROM for storing plural confidential data thereon address by address which has

no external direct input path and can be read only from an internal circuit inside of the

integrated circuit;

        a tester for testing the ROM address by address;

        a storage device, which is included in the ROM, for storing plural redundancy

check data address by address that have been obtained by performing a

predetermined calculation on each of the corresponding plural confidential data, the

plural redundancy check data an each of the corresponding plural confidential data

being stored at mutually different addresses on the ROM;

a checker for performing the same calculation as the predetermined calculation

on each of the plural confidential data that has been read out from the ROM address by

address;

a comparator for comparing a result of the calculation performed by the checker

to each of the corresponding plural redundancy check data stored in the storage device

address by address; and

an address decoder which enables an operation of the comparator if ~~the~~ an

address is for the redundancy check data, and disables the operation of the comparator

if the address is for the confidential data.

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5. A method for testing a semiconductor integrated circuit including a ROM that stores

plural confidential data thereon address by address and which can be read only from

an internal circuit inside of the integrated circuit, the method comprising the steps of:

a. storing plural redundancy check data, which have been obtained by

performing a predetermined calculation on each of the corresponding

plural confidential data, in a redundancy check data storage device

included in the ROM;

    b. reading ou each of the plural confidential data from the ROM address by

    address and performing the same calculation as the predetermined

    calculation on each of the plural confidential data read out; and

    c. reading out each of the corresponding plural redundancy check data from

    the storage device address by address and comparing a result of the

    calculation performed in the step b) to each of the corresponding plural

    redundancy check data read out,

    wherein the plural redundancy check data and each of the corresponding

    plural confidential data are stored at mutually different addresses on the

    ROM,

    and the comparison is enabled if ~~the~~ an address is for the redundancy

    check data, and disabled if the address if for the confidential data.

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Examiner's Statement of Reasons for Allowance

5. Claims 1 and 5 are allowed.

    The following is a statement of reasons for the indication of allowable subject matter.

6. Applicant's invention is directed towards a system and a method for testing a

    semiconductor integrated circuit including storing plural redundancy check data,

    which have been obtained by performing a predetermined calculation on each of the

    corresponding plural confidential data, in a redundancy check data storage device

included in the ROM; reading out each of the plural confidential data from the ROM
address by address and performing the same calculation as the predetermined
calculation on each of the plural confidential data read out; and reading out each of
the corresponding plural redundancy check data from the storage device address by
address and comparing a result of the calculation performed in the previous step to
each of the corresponding plural redundancy check data read out, wherein the plural
redundancy check data and each of the corresponding plural confidential data are
stored at mutually different addresses on the ROM.

7. The closest prior art Hartung et al. (U.S. Patent 4438512) discloses a tester that
   includes a checker and comparing the checker calculation with each of the
   corresponding plural CRC data that is stored in the storage device address by
   address and Admitted Prior Art (APA) teaches a ROM for storing plural confidential
   data thereon address by address.

8. However, neither Hartung et al. nor APA discloses that the comparison is enabled if
   an address is for the redundancy check data, and disabled if the address if for the
   confidential data.

9. Introducing these limitations would not have been obvious to one of ordinary skill in
   the art.

10. The prior art, fails to anticipate or fairly suggest the limitation of applicant's
    independent claims, in such a manner that a rejection under 35 U.S.C. 102 or 103
    would be proper. As a result the claimed invention is considered to be in condition
    for allowance as being novel and non-obvious over prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on statement of Reasons for Allowance".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter Poltorak whose telephone number is (571) 272-3840. The examiner can normally be reached from Monday through Thursday from 9:00 until 5:00, and every other Friday from 9:00 until 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571) 272-3799. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1600.

GILBERTO BARRON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

12/11/06